REMARKS

In response to the Office Action mailed July 14, 2003, claims 24, 26, 27, 30, 33, 35, 36, 38, 39 and 43 have been amended, and no claim has been cancelled or added. Accordingly, claims 24-43 are now active in this application, of which claims 24, 33 and 43 are independent.

Entry of the Amendments and Remarks is respectfully requested because entry of Amendment places the present application *in condition for allowance*, or in the alternative, better form for appeal. No new matters are believed to be added by these Amendments.

Based on the above Amendments and the following Remarks, Applicants respectfully request that the Examiner reconsider the outstanding objections and rejections and they be withdrawn.

Rejections Under 35 U.S.C. §112

In the Office Action, claims 24-43 have been rejected under 35 U.S.C. §112, second paragraph for indefiniteness. This rejection is respectfully traversed.

In this response, claims 24, 26, 27, 30, 33, 35, 36, 38, 39 and 43 have been amended to replace "first difference" and "second difference" with --first voltage difference-- and --second voltage difference--, respectively.

An example of the claimed "first voltage difference" and "second voltage difference" is shown in FIG. 6 of the present application. Particularly, FIG. 6(b) shows a slashed portion illustrating the voltage difference between the common voltage Vcom and the voltage Vpu applied to the pixel electrode. FIG. 6(b) further shows the voltage Vpu is influenced by the data voltage Vd1 and swings as shown by the actual voltage Va depending on the polarity of the data voltage Vd1 with respect to the common voltage Vcom.

Hence, Applicants believe that, upon this amendment, claims 24-43 particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, Applicants respectfully request that the rejection over claims 24-43 be withdrawn.

Rejections Under 35 U.S.C. §103

In the Office Action, claims 24-31 and 33-42 have been rejected under 35 U.S.C. §103(a) for being unpatentable over U. S. Patent No. 6,229,516 issued to Kim, *et al.* ("Kim") in view of U. S. Patent No. 5,093,655 issued to Tanioka, *et al.* ("Tanioka"). This rejection is respectfully traversed.

Independent claim 24 recites "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". An example of this claimed feature is shown in FIG. 6(a) to FIG. 6(d) of the present application.

FIG. 6(a) and FIG. 6(c) show the first data voltage Vd1 applied to the first gate line block and the second data voltage Vc1 applied to the second gate line block. These data voltages Vd1 and Vc1 influence the pixel voltages Vpu and Vpd applied to the pixel electrodes of the first and second gate line blocks, respectively. FIG. 6(b) and FIG. 6(d) shows the actual pixel voltages Va and Vb in the first and second gate line blocks, respectively, that are influenced by the first and second data voltages Vd1 and Vc1.

According to the present invention, the first data voltage Vd1 and the second data voltage Vc1 are controlled to influence the first voltage difference (i.e., the slashed portion) between the common voltage Vcom and the actual voltage Va in the first gate line block and the second voltage difference between the common voltage Vcom and the actual voltage Vb such that the

first voltage difference and the second voltage difference are simultaneously increased or decreased, as shown in FIG. 6(b) and 6(d). asdf

The Examiner is respectfully requested to particularly pay attention to *the slashed portions* shown in FIG. 6(b) and 6(d), which illustrate the *voltage differences* between the common voltages Vcom and the actual pixel voltages Va and Vb in the first and second gate line blocks, respectively. As shown therein, when the voltage difference of the first gate line block increases, the voltage difference of the second gate line black decreases. Also, when the voltage difference of the first gate line block decreases, the voltage difference of the second gate line block decreases.

The conventional method of applying data voltages to the different gate link blocks is shown in FIG. 2 of the present application, in which, when the voltage difference of the first gate line block increase, the voltage difference of the second gate line block decreases, and when the voltage difference of the first gate line block decreases, the voltage difference of the second gate line block increase. "This makes a big difference in the amounts of the light permeating the liquid crystal material in the pixels at the boundaries of the upper block and the lower block, which results in the inconsistent brightness on the boundaries. Eventually, this appears as undesired lines at the boundaries between the upper block and the lower block" (Specification, Page 7, Lines 12-18).

However, by "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference" as recited claim 24, "the bright on the boundaries becomes almost uniform" "since a difference in the amount of light permeating the light crystal material on the pixels of the boundaries is small" (Specification, Page 21, Lines 2-4). "Consequently, the line patterns

appearing on the boundaries of the upper and lower panels in the conventional method of driving the dual scan LCD disappears" (Specification, Page 21, Lines 5-7).

In the Office Action, the Examiner asserted that the claimed feature of "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference" is disclosed in column 4, lines 4-46 of Kim. This assertion is respectfully disagreed with.

Column 4, lines 4-36 of Kim is directed to a double gate line block structure, but does not even remotely suggest "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". Thus, it is submitted that Kim fails to disclose this claimed feature.

Tanioka discloses reversing the polarity of the picture signal in adjacent columns, but Tanioka does not disclose "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". Thus, the deficiency from Kim is not cured by the secondary reference to Tanioka.

Since none of the cited references discloses or suggests the claimed feature, it is submitted that independent claim 24 is patentable over Kim and Tanioka. Claims 25-31 that are dependent from claim 24 would be also patentable at least for the same reason.

Independent claim 33 recites "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". As previously argued, this claimed feature is not disclosed or suggested by Kim and Tanioka. Thus, it is submitted that claim 33 is patentable over these cited references. Claims 34-42 that are dependent from claim 33 would be also patentable at least for the same reason.

Accordingly, Applicants respectfully request that the rejection over claims 24-31 and 33-42 be withdrawn.

Claims 32 and 43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kim in view of Tanioka, further in view Japanese Patent Publication No. 03-125187 to Konoue, et al. ("Konoue"). This rejection is respectfully traversed.

Claim 32 ultimately stems from independent claim 24. As previously argued, claims 24 is patentable over Kim and Tanioka. Konoue is directed to inverting the scanning direction of each gate line block at its border as shown FIG. 2. however. Konoue does not disclose or suggest "controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". For this reason, it is submitted that claim 24 is still patentable over Kim, Tanioka and Konoue. Thus, claim 32 that is dependent from claim 24 would be also patentable.

Independent claim 43 recites "a data driver controlling the first data signal and the second data signal to simultaneously increase or decrease the first voltage difference and the second voltage difference". As previously argued, none of Kim, Taniok and Konue discloses or suggest this claimed feature. Thus, it is submitted that claim 43 is patentable over Kim, Taniok and Konue.

CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 24-43 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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